

Figure 14-9. PC/XT Sources of Hardware Interrupts (Reprinted by permission from "IBM BIOS Technical Reference" c. 1984 by International Business Machines Corporation)

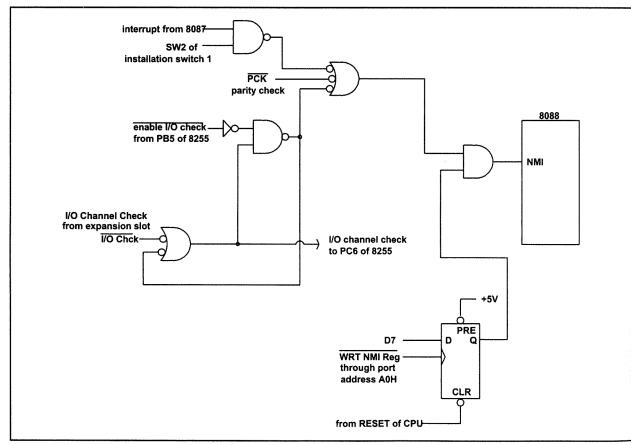


Figure 14-10. Sources of NMI in the PC/XT (Reprinted by permission from "IBM BIOS Technical Reference" c. 1984 by International Business Machines Corporation)

CHAPTER 14: INTERRUPTS AND THE 8259 CHIP

If the NMI is so important to the system, which devices can activate it, and can they be masked at all? First, as can be seen from Figure 14-10, there are three sources of activation of the NMI:

- 1. NPIRQ (numerical processor interrupt request)
- 2. Read/write PCK (parity check)
- 3. IOCHK (input/output channel check)

Since three different sources can activate NMI, how does the system know which one is requesting interrupt service at any given time? The IBM PC system recognizes which of these interrupt requests has been activated by checking input port C of the 8255. It looks at PC6 of the 8255 to see if it is IOCHK and at PC7 to see if it is PCK. The NMI service routine software must check PC6 and PC7 and determine which one has requested service. If neither of these two is requesting service, the request must have come from the 8087 coprocessor on the motherboard (in IBM terminology, planer). IBM BIOS checks the source of each and as it finds them, displays an appropriate messages on the video screen. The BIOS code is shown next.

E2C3 E2C3 E2C3 50 E2C4 E462 E2C6 A8C0 E2C8 7415	746 747 NMI_INT 748 749 750 751	ORG PROC PUSH IN TEST JZ	0E2C3H NEAR AX AL,PORT AL,0C0H D14	;SAVE ORIG CONTENTS OF AX _C ;PARITY CHECK? ;NO, EXIT FROM ROUTINE
E2CE A840 E2D0 7504 E2D6 	752 753 754 755 756 D13: 757	TEST JNZ 	AL,40H D13 	;ADDR OF ERROR MSG ;I/O PARITY CHECK ;DISPLAY ERROR MEG ;MUST BE PLANER sends the message to video and halts the system.
E2DF 58 E2E0 CF	762 D14: 763 764 765 NMI INTENDP	POP IRET	AX	;RESTORE ORIGINAL AX

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Is there any way that NMI can be masked? The answer is yes. As can be seen from Figure 14-10, NMI is masked by a RESET signal from the CPU with CLR of the D flip-flop when the computer is first turned on. It can also be unmasked or masked through port A0H by setting D7 of the data bus to 1 (unmask) or 0 (mask). Again from the IBM PC/XT BIOS we see the following:

	1261 1262	;	ENABLE NMI INTERRUPTS			
E5BC B080 E5BE E6A0	1263 1264	1263	MOV OUT	AL,80H 0A0H,AL	;ENABLE NMI INTERRUPTS	
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Review Questions

- 1. True or false. The IBM PC/XT uses only one 8259.
- 2. What ports are assigned to ICWs in the PC/XT?
- 3. In the PC/XT, the IRQ are (edge-, level-triggered).
- 4. Of the 256 possible interrupts of the 8088, which ones are assigned to IRQ0 IRQ7 of the 8259?
- 5. True or false. IRQ0 and IRQ1 can be used by the system but not by the user.
- 6. Which IRQ of the 8259 is available on the expansion slot?
- 7. True or false. The 80x86 can mask and unmask the NMI by using the STI and CLI instructions.
- 8. True or false. If there is a problem with the memory of the PC, NMI is activated.